System Level ESD Co-Design (Wiley - IEEE)

By Charvaka Duvvury;Harald Gossner

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Ajith Amerasekera and Charvaka Duvvury, Wiley, May 15, 2002. ESD LNA-ESD Co-Design for Simulation Methods for ESD Protection Development Harald Gossner,
http://emclab.mst.edu/emcbooks/

hardware/firmware co-design solution in an 8-bits microcontroller has been proposed to practically fix the system-level electrostatic discharge (ESD) systems
http://www.sciencedirect.com/science/article/pii/S0026271400002420

2 1 System Level ESD Design. real ESD controlled environments have a continuously reduced trend. The off-chip and on-chip system-level co-design meth-
http://link.springer.com/content/pdf/10.1007%2F978-3-319-03221-4_1.pdf

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Harald Gossner and Kaustav Banerjee. IEEE Transactions on Electron Charvaka Duvvury, IEEE International High Level Design Validation and Test
http://nrl.ece.ucsb.edu/publications/category

System-level ESD robustness is a because ground or VDD rails of the board can be involved in main discharge path of system-level ESD pulse. 4. Co-design concept
http://www.sciencedirect.com/science/article/pii/S0026271410004191

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The positive and negative gate-bias effect on ESD robustness of NMOS devices are analyzed respectively in this paper. The influence of gate-bias have been simulated
http://ieeexplore.ieee.org/search/freesearchresult.jsp?openedRefinements=*&filter=AND(NOT(4283010803))&rowsPerPage=100&queryText=(esd)&pageNumber=10
Duvvury, Charvaka (2 The application of co-design measures improves the ESD hardness EMI and increased the CDM failure level of a Class 0 ESD sensitive device
http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=4401722
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This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge (ESD) protection.
http://www.springer.com/us/book/9783319032207

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http://onlinelibrary.wiley.com/doi/10.1002/9781118703328.ch07/summary

System level ESD protection. The overall methodology for IC-system ESD co-design is presented as a step-by-step procedure that involves both ESD testing and
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